What is claimed is:

[Claim 1] 1. A method for performing read phase auto-calibration of a storage device, the method comprising:

writing data with at least one predetermined pattern into the storage device;
reading the data stored in the storage device by using at least one read phase of a plurality of read phases;
comparing the read data with the predetermined pattern; and
selecting a read phase from the plurality of read phases according to the comparing result.

[Claim 2]

2. The method of claim 1, wherein the plurality of read phases are relative to a reference signal.

[Claim 3] 3. The method of claim 2, wherein the reference signal is a strobe signal or a clock signal.

[Claim 4] 4. The method of claim 1, wherein the storage device is a dynamic random access memory (DRAM).

[Claim 5] 5. The method of claim 1, wherein the storage device is a double-data-rate (DDR) memory.

[Claim 6] 6. The method of claim 1, wherein the predetermined pattern is a hexadecimal number which can be equally transformed into to a binary number.

[Claim 7] 7. The method of claim 1, wherein the step of reading the data is to read the predetermined pattern stored in the storage device.

[Claim 8] 8. The method of claim 1, wherein the step of comparing is to check whether the data read from the storage device match the predetermined pattern.

[Claim 9] 9. The method of claim 1, wherein the read phase selected in the selecting step is determined from the phases without read error among the plurality of read phases.

[Claim 10] 10. The method of claim 1, wherein the step of selecting the read phase is to select a middle phase from consecutive phases without read error among the plurality of read phases.

[Claim 11] 11. The method of claim 10, wherein the position of the middle phase is at a center position or an approximately center position of the consecutive phases without read error.

[Claim 12] 12. A circuit for performing read phase auto-calibration of a storage device, the circuit comprising:

a control unit coupled to the storage device for determining a read phase among a plurality of read phases and outputting a multiplexing signal according to the determined read phase;
a delay chain for generating a plurality of delay signals; and
a multiplexer coupled to the control unit and the delay chain for selecting a delay signal among the delay signals according to the multiplexing signal.

[Claim 13] 13. The circuit of claim 12, wherein the control unit is a digital signal processor.

[Claim 14] 14. The circuit of claim 12, wherein the control unit is a firmware.

[Claim 15] 15. The circuit of claim 12, wherein the control unit reads the data stored in the storage device by using at least two of the read phases and compares the read data with the predetermined pattern, and determines the read phase according to the compared result.